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(11) **EP 1 265 466 A2** 

(12)

## **EUROPEAN PATENT APPLICATION**

(43) Date of publication:

11.12.2002 Bulletin 2002/50

(51) Int CI.7: **H05K 1/16**, H05K 3/46

(21) Application number: 02253836.7

(22) Date of filing: 31.05.2002

(84) Designated Contracting States: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR Designated Extension States:

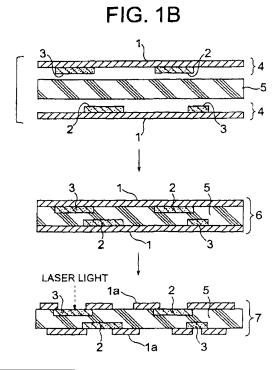
AL LT LV MK RO SI

(30) Priority: **05.06.2001 JP 2001170019 05.06.2001 JP 2001170020** 

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- (54) Method for fabrication wiring board provided with passive element and wiring board provided with passive element
- (57)A fabricating method of a wiring board provided with passive elements is disclosed. The fabricating method includes coating one or both of resistive paste and dielectric paste (2) on at least any one of first surfaces of a first metal foil and a second metal foil (1) each of which has a first surface and a second surface; arranging an insulating board (5) having thermo-plasticity and thermo-setting properties so as to face the first surface of the first metal foil (1), and arranging the first surface side of the second metal foil (1) so as to face a surface different from a surface to which the first metal foil (1) faces of the insulating board (5); forming a double-sided wiring board by stacking, pressurizing and heating the arranged first metal foil (1), insulating board (5), and second metal foil (1), and thereby integrating these; and patterning the first metal foil and/or the second metal foil (1).



#### Description

[0001] The present invention relates to a method for fabricating a wiring board provided with a passive element and to a wiring board provided with a passive element, in particular to a method for fabricating a wiring board provided with a passive element having an aptitude for improving characteristics of the passive element and to a wiring board provided with a passive element having an aptitude for improving characteristics of the passive element.

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[0002] As portable electronic devices become smaller in size, lighter in weight and thinner in thickness, smaller size chip components, such as L (inductor, coil), C (condenser, capacitor) and R (resistor), have been developed. Furthermore, by burying passive elements such as C and L in a wiring substrate, composite components have been developed. Such integration with a wiring substrate has been actively forwarded particularly in multi-layered ceramic substrates and adopted in, for instance, RF (radio frequency) modules for portable telephones.

[0003] A multi-layered ceramic substrate is fabricated by first preparing a necessary number of green sheets (ceramic material sheet before sintering) on which coil patterns and capacitor electrode patterns are formed by, for instance, printing a thick film of a conductive paste, followed by stacking these in a predetermined order and by performing simultaneous thermocompression bonding and sintering.

[0004] Furthermore, a plurality of green sheets having different dielectric constants is prepared, and according to characteristics of a passive component to be incorporated, the green sheets are appropriately selected. This is performed by selecting a low dielectric constant green sheet that can set a high self-resonant frequency and secure a high Q-value for a ceramic material that constitutes an inductor, and a high dielectric constant green sheet for a ceramic layer that forms a capacitor, respectively. By use of such a combination, an LC composite component having higher function may be incorporated.

[0005] In the aforementioned technique, ceramics is used for wiring substrate material. It is expected that in future an operating frequency of an RF circuit that is used in a portable telephone may reach 10 to 20 GHz. In view of this, it is important from a viewpoint of product costs and so on that organic resins having lower relative dielectric constants are made available as the substrate material. As things are, when an organic resin that is lower in dielectric constant than the ceramics is used as a substrate material (inter-layer insulating layer), and passive elements such as capacitors and so on are incorporated similarly to the multilayer ceramic substrate, it is supposed that an element area may become larger and desired characteristics may not be obtained.

[0006] Furthermore, as to the so-called hybrid multilayered substrates, there are the following reports. That

is, first, according to characteristics of a passive element to be incorporated, a substrate material in which a dielectric material and a magnetic material are mingled with polymer is prepared. Thus obtained substrate material is etched, and thereby a patterned capacitor layer and a coil layer are formed. These are laminated in a predetermined order, and thereby a hybrid multi-layered substrate is obtained.

[0007] However, in this technique, the multi-layered substrate may warp due to the difference of characteristics such as thermal expansion coefficient and so on between the substrate materials. In addition, since only one specified kind of passive element may be formed in one layer, a design allowance when the passive elements are arranged is low. That is, it is inappropriate in obtaining a smaller size due to tendency to an increase in the number of layers as a whole.

[0008] Furthermore, there is another multi-layered organic resin substrate in which resistive paste, dielectric paste, and conductive paste are sequentially printed to incorporate R, L and C. However, since the paste that can be used in this case is restricted to kinds that allow completing heat treatment at temperatures lower than the heat resistance temperature of an organic resin that is used as an insulating layer, the desired characteristics may not be obtained in some cases.

[0009] The present invention is carried out in consideration of the aforementioned situations. That is, the present invention provides a method for fabricating a wiring board that is provided with passive elements having improved characteristics, and a wiring board that is provided with such passive elements.

[0010] A method for fabricating a wiring board provided with a passive element according to the present invention includes coating a resistive paste and/or a dielectric paste on at least any one of first surfaces of a first metal foil and a second metal foil each of which has the first surface and a second surface; arranging an insulating board having thermo-plasticity and thermo-setting properties so as to face the first surface of the first metal foil, and arranging the first surface side of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil and thereby integrating these; and patterning the first metal foil and/or the second metal foil of the formed double-sided wiring board.

[0011] That is, resistive paste and dielectric paste are coated on a metal foil. Accordingly, these pastes can be heat-treated (such as, for instance, drying, sintering, and curing) irrespective of the heat resistance temperature of an insulating board. Thereafter, the metal foil having thus, for instance, heat-treated resistive element and dielectrics and the insulating board are laminated. Accordingly, a wiring board provided with passive elements having excellent characteristics can be obtained.

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[0012] Furthermore, another method for fabricating a wiring board provided with a passive element according to the present invention includes coating a resistive paste on a first surface of at least a first metal foil of the first metal foil and a second metal foil each of which has the first surface and a second surface; forming a substantially conical conductive bump on a resistive element formed of the coated resistive paste; arranging an insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil and thereby integrating these so that the formed conductive bump may penetrate through the insulating board and establish an electrical contact and/or a heat conductive contact with the second metal foil; and patterning the first metal foil and the second metal foil of the formed double-sided wiring board.

**[0013]** That is, a resistive paste is coated on a metal foil. Accordingly, the heat-treatment (such as, for instance, drying, sintering, and curing) and so on of the paste can be performed irrespective of the heat resistance temperature of an insulating board. Thereafter, the metal foil having thus, for instance, heat-treated paste (resistive element) and the insulating board are laminated. Accordingly, a wiring board provided with passive elements (resistors in this case) having excellent characteristics can be obtained.

[0014] Furthermore, in this case, the wiring board may be configured so that the conductive bump may directly establish one or both of an electrical contact and a heat conductive contact with the coated/formed resistive element. Accordingly, since a lead wire can be pulled out of the resistive element while avoiding a contact between the resistive element and the metal foil, the resistive paste that is less compatible with a metal (for instance, copper) that is used for the metal foil may be used. Accordingly, by further expanding a range of choice of available resistive pastes, a wiring board provided with a passive element having excellent characteristics may be obtained. Furthermore, when the conductive bump is brought into a heat conductive contact with the resistive element, for instance, a heat sink may be disposed on a rear surface side (an opposite side from a surface side having a resistor thereon) of the insulating board.

[0015] Still furthermore, still another method for fabricating a wiring board provided with a passive element according to the present invention includes coating a dielectric paste on a first surface of at least a second metal foil of a first metal foil and the second metal foil each of which has the first surface and a second surface; coating a conductive paste so as to include on the coated dielectric paste and extend onto the first surface on

which the dielectric paste is coated; arranging an insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil and thereby integrating these; and patterning at least the second metal foil of the formed double-sided wiring board.

[0016] That is, a dielectric paste is coated on a metal foil. Accordingly, heat-treatment (such as, for instance, drying, sintering, and curing) and so on of the paste can be performed irrespective of the heat resistance temperature of an insulating board. Thereafter, the metal foil having thus, for instance, heat-treated paste (dielectric material) and the insulating board are laminated. Accordingly, a wiring board provided with a passive element (capacitor in this case) having excellent characteristics can be obtained.

**[0017]** Furthermore, in this case, furthermore, an electrical conductor formed of the conductive paste and the metal foil may sandwich dielectrics, thereby a so-called parallel plate capacitor is formed. Thereby, a capacitor having higher capacitance may be formed.

[0018] Still furthermore, still another method for fabricating a wiring board provided with a passive element according to the present invention includes coating a dielectric paste on a first surface of at least a second metal foil of a first metal foil and the second metal foil each of which has the first surface and a second surface; coating a first conductive paste so as to contain on the coated dielectric paste and to extend onto the first surface on which the dielectric paste is coated; coating a second dielectric paste so as to contain on the coated first conductive paste; coating a second conductive paste so as to contain on the coated second dielectric paste, to extend onto the first surface on which the second dielectric paste is coated, and not to come into contact with the first conductive paste; arranging an insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil, and thereby integrating these; and patterning at least the second metal foil of the formed double-sided wiring board.

[0019] That is, a dielectric paste and a conductive paste are coated on a metal foil. Thereby, heat treatment (for instance, drying, sintering, and curing) of the pastes may be performed irrespective of the heat resistance temperature of an insulating board. Since the metal foil having thus, for instance, heat-treated paste (dielectric material) is laminated together with the insulating board,

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a wiring board provided with a passive element (capacitor in this case) excellent in characteristics can be obtained.

**[0020]** In this case, furthermore, since an electrical conductor made of the conductive paste and the metal foil may be formed to sandwich the dielectrics, and the electrical conductor and an electrical conductor made of the second conductive paste may be formed to sandwich the second dielectrics, a so-called parallel plate capacitor may be formed in multi-layers. Thereby, a capacitor having higher capacitance may be formed. Such a multi-layered capacitor, by forming dielectrics and an electrical conductor in a further multi-layered structure due to the dielectric paste and conductive paste, may be provided with furthermore higher capacitance.

[0021] Furthermore, still another method for fabricating a wiring board provided with a passive element according to the present invention includes forming a substantially conical conductive bump on a first surface of a first metal foil having the first surface and a second surface; forming a substantially conical magnetically permeable bump on a first surface of a second metal foil having the first surface and a second surface; arranging an insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface side of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil, and thereby integrating these so that the formed conductive bump and magnetically permeable bump may penetrate through the insulating board and establish a contact with the first or second metal foil; and patterning the first metal foil and the second metal foil of the formed double-sided wiring board.

[0022] That is, a conductive bump and a magnetically permeable bump are formed on a metal foil. Accordingly, the bumps can be heat-treated (such as, for instance, drying, sintering, and curing) irrespective of the heat resistance temperature of an insulating board. Thereafter, the metal foil having thus, for instance, heat-treated bump and the insulating board are laminated. Accordingly, a wiring board provided with a passive element (in this case inductor) having excellent characteristics may be obtained.

**[0023]** Furthermore, in this case, furthermore, due to patterning of a first and second metal layers and due to an electrical connection between these by means of a conductive bump, a helical inductor with the magnetically permeable bump as a core may be formed. Accordingly, ones having larger inductance may be formed.

**[0024]** A wiring board provided with a passive element according to the present invention includes an insulating board having a first surface and a second surface; a layered resistive element and/or a layered dielectrics disposed on the first surface and/or the second surface of

the insulating board so as to sink in a thickness direction of the insulating board; and a first wiring layer and a second wiring layer that are, respectively, disposed on the first surface and the second surface of the insulating board, and each of which has a connection with the layered resistive element/the layered dielectrics disposed on the corresponding first surface/second surface.

[0025] Furthermore, another wiring board provided with a passive element according to the present invention includes an insulating board having a first surface and a second surface; a layered resistive element disposed on the second surface of the insulating board so as to sink in a thickness direction of the insulating board; a first and second wiring layers disposed on the first surface and second surface of the insulating board, respectively; and a conductive bump that penetrates through the insulating board and is in an electrical connection and/or a heat conductive connection with the layered resistive element and the first wiring layer.

[0026] Still furthermore, still another wiring board provided with a passive element according to the present invention includes an insulating board having a first surface and a second surface; a layered electrical conductor disposed on the second surface of the insulating board so as to sink in a thickness direction of the insulating board; a layered dielectrics disposed in partial contact with a top surface of the layered electrical conductor so as to sink in a thickness direction of the insulating board; and a wiring layer that is disposed on the second surface of the insulating board and has individual connections with the layered electrical conductor and the layered dielectrics.

[0027] Furthermore, still another wiring board provided with a passive element according to the present invention includes an insulating board having a first surface and a second surface; a first and second wiring layers, respectively, disposed on the first surface and the second surface of the insulating board; a conductive bump that penetrates through the insulating board and is in an electrical connection with the first wiring layer and the second wiring layer; and a magnetically permeable bump that penetrates through the insulating board. In the above, the first wiring layer has a first pattern that surrounds the magnetically permeable bump, the second wiring layer has a second pattern that surrounds the magnetically permeable bump, and the first and second patterns are in an electrical continuity due to the conductive bump.

[0028] The wiring boards are ones that can be fabricated by the aforementioned respective fabricating methods.

**[0029]** The invention is described with reference to the drawings, which are presented for the purpose of illustration only and do not limit the scope of the invention.

Fig. 1A and Fig. 1B are diagrams showing a process for fabricating a double-sided wiring board accord-

ing to a fabricating method according to an embodiment of the present invention.

Fig. 2A and Fig. 2B are diagrams showing a process for fabricating a double-sided wiring board according to a fabricating method according to another embodiment of the present invention.

Fig. 3 is a perspective view showing an example of the double-sided wiring board fabricated by the process shown in Fig. 1A and Fig. 1B, or Fig. 2A and Fig. 2B.

Fig. 4A and Fig. 4B are diagrams showing a process for making the double-sided wiring board that is fabricated by the process shown in Fig. 1A and Fig. 1B, or Fig. 2A and Fig. 2B into a material of a three-layered or four-layered material.

Fig. 5A and Fig. 5B are diagrams showing a metal foil necessary when the three-layered wiring board or four-layered wiring board is fabricated by use of the double-sided wiring board that is fabricated by the process shown in Fig. 1A and Fig. 1B, or Fig. 2A and Fig. 2B, and a process applied thereon. Fig. 6 includes diagrams showing a process for fabricating the four-layered wiring board by use of a

ricating the four-layered wiring board by use of a wiring board material that is fabricated by the process shown in Fig. 4A and Fig. 4B, and the metal foil shown in Fig. 5A and Fig. 5B.

Fig. 7 includes perspective views showing the process shown in Fig. 6.

Fig. 8 is a perspective view showing the four-layered wiring board fabricated according to the fabricating method shown in Fig. 6 (Fig. 7) and having a loop antenna in an outer wiring.

Fig. 9 is a partial sectional view as an example of a double-sided wiring board fabricated according to the fabricating method according to still another embodiment of the present invention.

Fig. 10 is a bottom view of the double-sided wiring board shown in Fig. 9.

Fig. 11 is a partial sectional view showing another example to the example shown in Fig. 9.

Fig. 12A and Fig. 128 are partial sectional views for explaining an example of a double-sided wiring board fabricated according to the fabricating method according to still another embodiment of the present invention.

Fig. 13A and Fig. 13B are partial sectional views for explaining another example to the example shown in Fig. 12A and Fig. 12B.

Fig. 14A and Fig. 14B are diagrams for explaining irregularity in the shape at a periphery of the dielectrics/resistive element/electrical conductor coated on the metal foil and an improvement thereof.

Fig. 15A and Fig. 15B are diagrams for explaining an example of a four-layered wiring board fabricated according to the fabricating method according to still another embodiment of the present invention. Fig. 16A and Fig. 16B are diagrams for explaining another example to the example shown in Fig. 15A

and Fig. 15B.

[0030] The fabricating method according to the present invention, as an implementation mode, further includes forming a substantially conical conductive bump on the first surface of the first metal foil. In this case, the forming a double-sided wiring board is performed so that the formed conductive bump may penetrate through the insulating board and establish an electrical contact with the second metal foil. That is, since wiring layers on both sides are electrically connected by means of a conductive bump, the number of the processes may be reduced and a double-sided wiring board whose wiring layers on both sides have an electrical continuity may be easily fabricated.

**[0031]** Furthermore, in an implementation mode of the fabricating method according to the present invention, the patterning the first metal foil and/or the second metal foil includes the formation of an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern. That is, an inductor and a loop antenna are formed by patterning a metal foil.

[0032] Still furthermore, the fabricating method according to the present invention further includes trimming a resistor formed from the resistive paste by use of the patterned first metal foil and/or the patterned second metal foil as an electrode. That is, since an electrode can be formed to a resistor due to the patterning, by making use thereof for resistance measurement, is the resistor trimmed.

**[0033]** Furthermore, in an implementation mode of the fabricating method according to the present invention, the coating the resistive paste and/or the dielectric paste includes removing a periphery portion thereof after the coating. By removing irregularity at the edge portions of the coated resistive element and dielectrics, the resistor and capacitor having higher accuracy may be obtained.

[0034] Still furthermore, the fabricating method according to the present invention, as an implementation mode, further includes forming a substantially conical conductive bump on a first surface of a third metal foil having the first surface and a second surface; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, and arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface that faces the third metal foil of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged third metal foil, second insulating board, and double-sided wiring board, and thereby integrating these so that the conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil; and patterning the third metal foil of the formed three-layered wiring board.

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**[0035]** That is, by use of a double-sided wiring board as a material, and by further establishing an interlayer connection with a third wiring layer due to a conductive bump, a three-layered wiring board is fabricated.

[0036] Still furthermore, the fabricating method according to the present invention, as an implementation mode, further includes coating a resistive paste and/or a dielectric paste on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical conductive bump on the first surface of the third metal foil; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, and arranging a first metal foil side of the doublesided wiring board so as to face a surface different from a surface that faces the third metal foil of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged third metal foil, second insulating board, and double-sided wiring board, and thereby integrating these so that the conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil; and patterning the third metal foil of the formed three-layered wiring board.

**[0037]** That is, by use of a double-sided wiring board as a material, by further establishing an interlayer connection with a third wiring layer due to a conductive bump, a three-layered wiring board is fabricated. Here, a passive element may be enabled to use in the third wiring layer.

[0038] Furthermore, the fabricating method according to the present invention, as an implementation mode, further includes forming a substantially conical conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the conductive bump of the double-sided wiring board is formed, and arranging a third metal foil so as to face a surface different from a surface that faces the doublesided wiring board of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged double-sided wiring board, second insulating board, and third metal foil, and thereby integrating these so that the conductive bump formed on the double-sided wiring board may penetrate through the second insulating board and establish an electrical contact with the third metal foil; and patterning the third metal foil of the formed three-layered wiring board.

**[0039]** Also in this case, with a double-sided wiring board as a material, by further use of a conductive bump, an interlayer connection with a third wiring board is established, thereby forming a three-layered wiring board.

[0040] Still furthermore, the fabricating method according to the present invention, as an implementation

mode, further includes coating a resistive paste and/or a dielectric paste on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical conductive bump on the second surface of the second metal foil of the formed doublesided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the conductive bump of the double-sided wiring board is formed, and arranging the first surface side of the third metal foil so as to face a surface different from a surface that faces the doublesided wiring board of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged double-sided wiring board, second insulating board, and third metal foil, and thereby integrating these so that the conductive bump formed on the double-sided wiring board may penetrate through the second insulating board and establish an electrical contact with the third metal foil; and patterning the third metal foil of the formed three-layered wiring board.

**[0041]** In this case too, by use of a double-sided wiring board as a material, by further establishing an interlayer connection with a third wiring layer due to a conductive bump, a three-layered wiring board is fabricated. Here, a passive element may be enabled to use in the third wiring layer.

**[0042]** Furthermore, in an implementation mode of the fabricating method according to the present invention, the patterning the third metal foil includes the formation an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern. That is, by patterning the third metal foil, an inductor and a loop antenna may be formed.

[0043] Still furthermore, in an implementation mode of the fabricating method of the present invention, the coating a resistive paste and/or a dielectric paste on the first surface of the third metal foil includes removing a periphery portion thereof after the coating. This is a process to obtain a resistive element and dielectrics having higher accuracy from a resistive paste and dielectric paste coated on a third metal foil.

[0044] Furthermore, the fabricating method according to the present invention, as an implementation mode, further includes forming a substantially conical conductive bump on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical second conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the second conductive bump is

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formed of the double-sided wiring board, and arranging the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board; forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil, and thereby integrating these so that the conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil and the second conductive bump formed on the double-sided wiring board may penetrate through the third insulating board and establish an electrical contact with the fourth metal foil; and patterning the third metal foil and/ or the fourth metal foil of the formed four-layered wiring board.

[0045] That is, by use of a double-sided wiring board as a material, by establishing an interlayer connection between the third and fourth wiring layers due to a conductive bump, a four-layered wiring board is fabricated. [0046] Still furthermore, the fabricating method according to the present invention, as an implementation mode, further includes coating a resistive paste and/or a dielectric paste on at least any one of first surfaces of a third and fourth metal foils each of which has the first surface and a second surface; forming a substantially conical conductive bump on the first surface of the third metal foil; forming a substantially conical second conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the second conductive bump is formed of the double-sided wiring board, and arranging the first surface side of the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board; forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, doublesided wiring board, third insulating board, and fourth metal foil, and thereby integrating these so that the conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil and the second conductive bump formed on the double-sided wiring board may penetrate through the third insulating board and establish an electrical contact with the fourth metal foil; and patterning the third metal foil and/or the fourth metal foil of the formed four-layered wiring board.

[0047] Also in this case, by use of a double-sided wiring board as a material, by further establishing an inter-

layer connection with a third and fourth wiring layer due to a conductive bump, a four-layered wiring board is fabricated. Even in the third and fourth wiring layers, passive elements may be utilized.

**[0048]** Furthermore, in an implementation mode of the fabricating method according to the present invention, the patterning the third metal foil and/or the fourth metal foil includes the formation of an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern. That is, by patterning a third metal foil and a fourth metal foil, an inductor and a loop antenna may be formed.

[0049] Still furthermore, in an implementation mode of the fabricating method of the present invention, the coating a resistive paste and/or a dielectric paste on at least any one of the first surfaces of the third and fourth metal foils includes removing a periphery portion thereof after the coating. This is a process for obtaining a resistive element and/or dielectrics having higher accuracy from the resistive paste and the dielectric paste coated on the third metal foil and/or the fourth metal foil.

[0050] Furthermore, the fabricating method according to the present invention, as an implementation mode, further includes forming a substantially conical second conductive bump on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical second magnetically permeable bump on a first surface of a fourth metal foil having the first surface and a second surface; forming a substantially conical third conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; forming a substantially conical third magnetically permeable bump on a surface of the first metal foil side of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging a first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the third conductive bump is formed of the double-sided wiring board, and arranging the first surface side of a fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board; forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, doublesided wiring board, third insulating board, and a fourth metal foil, and thereby integrating these so that the second conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil, the second magnetically permeable bump formed on the double-sided wiring board may penetrate through the second insulating board and establish a contact with the third metal foil, the third conductive bump formed on the

double-sided wiring board may penetrate through the third insulating board and establish an electrical contact with the fourth metal foil, and the third magnetically permeable bump formed on the fourth metal foil may penetrate through the third insulating board and establish a contact with a surface of the second metal foil side of the double-sided wiring board; and patterning the third metal foil and the fourth metal foil of the formed four-layered wiring board.

**[0051]** That is, by use of a magnetically permeable bump as a core, a helical inductor is attempted to form in the four-layered wiring board.

**[0052]** Furthermore, the fabricating method according to the present invention, as an implementation mode, further includes forming a through-hole in a formed double-sided wiring board and filling a magnetically permeable material in the formed through-hole. In place of the magnetically permeable bump, a pillar-like body formed by filling a magnetically permeable material in a through-hole may be used as a core of a helical inductor.

[0053] Furthermore, the fabricating method according to the present invention is a fabricating method of a wiring board provided with a passive element that, as an implementation mode, further includes forming a substantially conical conductive bump on the first surface of the first metal foil, and the forming a double-sided wiring board is performed so that the formed conductive bump may penetrate through the insulating board and establish an electrical contact with the second metal foil. The present fabricating method further includes forming a substantially conical second conductive bump on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical third conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermoplasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the third conductive bump is formed of the double-sided wiring board, and arranging the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board; forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil, and thereby integrating these so that the second conductive bump formed on the third metal foil may penetrate through the second insulating board and establish an electrical contact with the first metal foil and the third conductive bump formed on the double-sided wiring board may penetrate through the third insulating board and establish an electrical contact with the fourth metal

foil; patterning the third metal foil and the fourth metal foil of the formed four-layered wiring board; forming a through-hole in the formed four-layered wiring board; and filling a magnetically permeable material in the formed through-hole.

**[0054]** In this case too, in place of the magnetically permeable bump, a pillar-like body that is formed by filling a magnetically permeable material in a through-hole is attempted to use as a core of a helical inductor. The wiring board has a four-layered wiring layer.

[0055] Furthermore, the wiring board according to the present invention, as an implementation mode, further includes a conductive bump that penetrates through the insulating board, wherein each of the first and second wiring layers has an electrical connection with the conductive bump. That is, since the electrical connection between the wiring layers on both sides is performed by use of a conductive bump, the present wiring board is a wiring board whose both wiring layers have an electrical continuity and enables to reduce the number of processes, that is, to realize higher productivity.

**[0056]** Furthermore, as an implementation mode of the wiring board according to the present invention, at least one of the first and second wiring layers has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern. That is, an inductor and a loop antenna are formed as a metal foil pattern.

[0057] Still furthermore, a wiring board according to the present invention, as an implementation mode, further includes a second insulating board disposed in contact with the first wiring layer side of the insulating board; a conductive bump that penetrates through the second insulating board; and a third wiring layer disposed on a side different from the insulating board side of the second insulating board; wherein the first wiring layer of the insulating board is disposed so as to sink in a thickness direction of the second insulating board; and each of the first and third wiring layers has an electrical connection with the conductive bump. This is a three-layered wiring board that contains a double-sided wiring board inside thereof and in which an interlayer connection with a third wiring layer is established by means of a conductive bump.

[0058] Still furthermore, a wiring board according to the present invention, as an implementation mode, further includes a second layered resistive element and/or a second layered dielectrics disposed on the third wiring layer side of the second insulating board so as to sink in a thickness direction of the second insulating board; wherein the third wiring layer has a connection with the second layered resistive element/the second layered dielectrics. Thereby, a passive element is made available even in a third wiring layer.

**[0059]** Furthermore, as an implementation mode of a wiring board according to the present invention, the third wiring layer has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-

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like due to a pattern. That is, an inductor and a loop antenna are formed as a metal foil pattern.

[0060] Still furthermore, a wiring board according to the present invention further includes, as an implementation mode, a third insulating board disposed in contact with the second wiring layer side of the insulating board; a second conductive bump that penetrates through the third insulating board; and a fourth wiring layer disposed on a side different from the insulating board side of the third insulating board; wherein the second wiring layer of the insulating board is disposed so as to sink in a thickness direction of the third insulating board; and each of the second and fourth wiring layers has an electrical connection with the second conductive bump. This is a four-layered wiring board that contains a doublesided wiring board as a core wiring board and in which interlayer connections with third and fourth wiring layers are further implemented by means of conductive bumps.

**[0061]** Still furthermore, a wiring board according to the present invention further includes, as an implementation mode, a second layered resistive element and/or a second layered dielectrics disposed on the fourth wiring layer side of the third insulating board so as to sink in a thickness direction of the third insulating board; wherein the fourth wiring layer has a connection with the second layered resistive element/the second layered dielectrics. Thereby, a passive element is made available even in third and fourth wiring layers.

[0062] Furthermore, as an implementation mode of a wiring board according to the present invention, the fourth wiring layer has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern. That is, an inductor and a loop antenna are formed as a metal foil pattern. [0063] Still furthermore, a wiring board according to the present invention further includes, as an implementation mode, a second layered dielectrics disposed under a bottom surface of the layered electrical conductor and a second electrical conductor that is disposed including under the bottom surface of the second layered dielectrics and is brought into contact with the wiring layer. That is, the present wiring board includes a multilayered parallel plate capacitor.

[0064] Furthermore, a wiring board according to the present invention, as an implementation mode, further includes a second insulating board disposed on the first wiring layer side of the insulating board; a third insulating board disposed on the second wiring layer side of the insulating board; a third wiring layer disposed on a different surface side from the insulating board of the second insulating board; a fourth wiring layer disposed on a different surface side from the insulating board of the third insulating board; a second conductive bump that penetrates through the second insulating board and is brought into electrical connections with the first wiring layer and the third wiring layer; a second magnetically permeable bump that penetrates through the second in-

sulating board; a third conductive bump that penetrates through the third insulating board and is brought into electrical connections with the second wiring layer and the fourth wiring layer; and a third magnetically permeable bump that penetrates through the third insulating board; wherein the first wiring layer is disposed so as to sink in a thickness direction of the second insulating board; the second wiring layer is disposed so as to sink in a thickness direction of the third insulating board; the magnetically permeable bump, the second magnetically permeable bump and the third magnetically permeable bump are disposed in series; the third wiring layer has a third pattern that surrounds the second magnetically permeable bump; the fourth wiring layer has a fourth pattern that surrounds the third magnetically permeable bump; the first and third patterns are in an electrical continuity due to the second conductive bump; and the second and fourth patterns are in an electrical continuity due to the third conductive bump.

**[0065]** That is, by use of a magnetically permeable bump as a core, a helical inductance is formed in a four-layered wiring board.

[0066] Furthermore, a wiring board according to the present invention includes, as an implementation mode, in place of the magnetically permeable bump, the second magnetically permeable bump, and the third magnetically permeable bump, a pillared body that has a magnetically permeable material and penetrates through the insulating board, the second insulating board, and the third insulating board. That is, in place of a magnetically permeable bump as a core, a pillar having a magnetically permeable material is used as a core of a helical inductor.

[0067] In the following, embodiments of the present invention will be explained with reference to the drawings. Fig. 1A and Fig. 1B are diagrams showing a process for fabricating a double-sided wiring board according to one embodiment of the present invention.

[0068] First, as shown in Fig. 1A upper side, a metal foil (a copper foil, for instance) 1 is prepared. On this metal foil 1, a dielectric paste is coated to be dielectrics 2 of a passive element (capacitor) necessary as a wiring board. Although a coating method is not particularly restricted, when, for instance, a screen-printing is used, over an entire surface, as many as necessary may be coated with high productivity and relatively high accuracy. As a dielectric paste, for instance, a composite in which powder of barium titanate, a high dielectric material is dispersed in a resinouos binder may be used. As an example, a dielectric paste CX-16, which is commercially available from ASAHI Kagaku Kenkyusho, may be utilized.

**[0069]** Furthermore, on the metal foil 1, a resistive paste is coated to be a resistive element 3 of a passive element (resistor) necessary as a wiring board. The coating method of the resistive paste is also identical as that mentioned above. As a resistive paste, for instance, a composite in which resistive material powder is dis-

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persed in a resinouos binder may be used. As an example, resistive pastes TU-15-8, TU-50-8, or TU-100-8, which are commercially available from ASAHI Kagaku Kenkyusho, may be utilized.

**[0070]** It is generally better to separately coat a dielectric paste and a resistive paste followed by separately drying and so on. It is because after the drying, a former coating state, without being interfered, may be maintained. The processing such as the drying and so on may be performed, irrespective of a heat resistance temperature of an insulating board (organic material) to be referred to later, at temperatures adequate for processing each of the dielectric paste and the resistive paste. Accordingly, since a range of choice of kinds thereof is wide, it contributes in the formation of a passive element having higher accuracy.

[0071] Furthermore, in order to make the resistive element 3 furthermore accurate, a method (post-treatment) as shown in Fig. 14A and Fig. 14B may be used. Fig. 14A and Fig. 14B are diagrams for explaining irregularity in the shape at a periphery portion of the resistive element (/dielectrics/electrical conductor) formed on a metal foil and an improvement thereof. Fig. 14A is a sectional view and Fig. 14B is a top view thereof.

[0072] In the resistive element 3 coated by means of the screen-printing and so on, in general, as shown in Fig. 14A, a shape, such as a thickness at the periphery thereof is formed a little differently from that of an inside portion (edge effect). Such a thickness variation may cause irregularity in a sheet resistance value (one of characteristic value of a resistive element; a resistance value between opposite sides of a square). Accordingly, edge portions 30 of the resistive element 3 are removed when the resistive element 3 is formed on the metal foil 1. In such removal, for instance, laser beam may be used. Since, due to such the removal, a thickness is more homogenized, a resistive element having a resistance value closer to that expected from the sheet resistance value may be formed. In the case of the dielectrics 2, accuracy is obtained similarly.

**[0073]** As mentioned above, a coated and formed metal foil 4 on a surface of which the resistive element 3 and the dielectrics 2 are formed is formed. Next, as shown in Fig. 1B upper side, resistive element 3/dielectrics 2 sides of two coated and formed metal foils 4 are arranged at a predetermined position necessary as a wiring board so as to face both sides of a prepreg to be an insulating board 5. The prepreg is obtained by impregnating a curable resin such as, for instance, epoxy resin in a reinforcing material such as glass fiber. Before curing, it is in a semi-cured state and has thermo-plasticity and thermo-setting properties.

[0074] Next, as shown in Fig. 1B center, three, that is, the coated/formed metal foil 4, insulating board 5 and another coated/formed metal foil 4 are stacked, pressurized and heated and thereby integrating these, a double-sided wiring board 6 is obtained. In the double-sided wiring board 6, the dielectrics 2 and the resistive ele-

ment 3 are integrated so as to sink in a thickness direction of the insulating board 5. This is due to the thermoplasticity and thermo-setting properties of the prepreg to be the insulating board 5.

[0075] Next, as shown in Fig. 1B lower side, the metal foils 1 on both sides are patterned into patterns 1a necessary as a wiring board. Due to the patterning, a double-sided wiring board 7 on which at least both end electrodes of the dielectrics 2 and the resistive element 3 are formed may be obtained. In the patterning, existing methods such as, for instance, the formation of a mask due to coating of photo-resist and exposure thereof, etching of the metal foil 1 due to the mask, and so on may be used.

**[0076]** In addition, the resistive element 3 may be trimmed by use of the both end electrodes formed by the patterning as resistance value measuring terminals. The trimming is a process in which, for instance, by use of laser light, the resistive element 3 is partially burned and brought to conform to a predetermined resistance value.

[0077] Although processes following the above are not shown in the drawings, the formation of solder resist and plating layers including on the pattern 1a, mounting of surface-mounting components on the pattern 1a, or flip-chip mounting of semiconductor chips may be implemented according to existing methods. Furthermore, as well known, a through-hole is bored in a double-sided wiring board 7, a conductive layer is formed on an internal surface thereof, and thereby the double-sided wiring board 7 having an electrical continuity between both wiring layers thereof may be formed. Still furthermore, according to the aforementioned etching of the metal foil 1, a vortical inductor may be formed. In this case, such a through-hole may be utilized as an inside terminal.

[0078] In the aforementioned embodiments, since materials are selected from a wide range of choice and the dielectrics 2 and the resistive element 3 are previously formed from the selected materials on the metal foil 1, on the same layer, a capacitor and resistor excellent in characteristics may be formed in a mingled state. Furthermore, since an organic material is used as the insulating board 5, lighter weight may be realized than in the case of ceramics.

45 [0079] In the aforementioned explanation, each of the dielectrics 2 to be a capacitor, and the resistive element 3 to be a resistor is formed by coating a paste-like composite. However, other than this, when a vortical inductor is formed, a conductive paste may be previously coated vortically as a paste-like composite on a metal foil 1.

[0080] Next, a process for fabricating a double-sided wiring board according to a fabricating method according to another embodiment of the present invention will be explained with reference to Fig. 2A and Fig. 2B. Fig. 2A and Fig. 2B are diagrams showing a process for fabricating a double-sided wiring board according to a fabricating method according to another embodiment of the

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present invention. The same regions as Fig. 1A and Fig. 1B are given the same reference numerals. Explanation of the same regions will be omitted.

[0081] This embodiment is different from one shown in Fig. 1A and Fig. 1B in that as shown in Fig. 2A lower side, a process in which the coated/formed metal foil 4 is transformed into a conductive bump formed metal foil 4a on which conductive bumps 8 have been formed is added

[0082] The conductive bump 8 may be formed on a place necessary as a wiring board on the coated/formed metal foil 4a by means of, for instance, screen printing. For this, as a conductive paste, for instance, one that is prepared by dispersing metal particles (silver, gold, copper, solder and so on) in a paste-like resin followed by mixing a volatile solvent is coated on the metal foil 4 by means of screen printing. The conductive bump 8 is necessary to have a height enough to penetrate through the insulating board 5 as will be detailed later. Accordingly, the conductive bump 8 is forced to have a substantially conical shape as a whole.

**[0083]** After the conductive bump formed metal foil 4a is obtained as shown in the above, next, as shown in Fig. 2B upper side, a resistive element 3 and dielectrics 2 side of the coated/formed metal foil 4 is disposed so as to face one side of both sides of the prepreg to be a insulating board 5, and a resistive element 3, dielectrics 2 and conductive bump 8 side of the conductive bump formed metal foil 4a is disposed so as to face the other side of both sides of the prepreg.

[0084] Next, as shown in Fig. 2B center, a double-sided wiring board 6a is obtained by stacking, pressurizing and heating three, that is, the coated/formed metal foil 4, insulating board 5, and conductive bump formed metal foil 4a, and thereby integrating these. In the double-sided wiring board 6a, the dielectrics 2 and resistive element 3 are integrated so as to sink in a thickness direction of the insulating board 5, and the conductive bump 8 penetrates through the insulating board 5 and comes into an electrical contact with the opposing metal foil 1. Such a state is realized because, as mentioned above, the insulating board 5 had thermo-plasticity and thermo-setting properties, and the conductive bump 8 is originally formed into a substantial cone.

[0085] In the double-sided wiring board 6a, since an electrical continuity between both wiring layers is established by the conductive bump 8, there is no need of a further process such as the formation of a through-hole to establish an electrical continuity between both wiring layers. Accordingly, since a space for the formation of the through-hole is not necessary, a wiring board of higher density may be obtained. Furthermore, in the integrating process, since a pressure on the dielectrics 2 and the resistive element 3 may be alleviated by the conductive bump 8 that works as a support, there is an advantageous effect that dispersions of various characteristics of the dielectrics 2 and the resistive element 3 that are caused at the integration may be suppressed.

[0086] Following the above, as shown in Fig. 2B lower side, the metal foils 1 on both sides are patterned into a pattern 1a necessary as a wiring board (substantially similar to the case of Fig. 1B lower side). Due to the patterning, a double-sided wiring board 7a in which both end electrodes of the dielectrics 2 and the resistive element 3 are at least formed may be obtained. In addition to this, the resistive element 3 may be trimmed by use of the both end electrodes formed by this patterning as resistance value measurement terminals. This is also as explained above.

[0087] Furthermore, although the processes following the above are not shown in the drawings, the formation of solder resist and plating layers including on the pattern 1a, mounting of surface-mounting components on the pattern 1a, or flip-chip mounting of semiconductor chips and so on may be performed according to existing methods. Still furthermore, according to the etching of the metal foil 1 as mentioned above, a vortical inductor may be formed. In this case, the above-explained conductive bump 8 may be utilized as an inside terminal.

[0088] In the above-explained embodiment, similarly

to the embodiment explained embodiment, similarly to the embodiment explained in Fig. 1A and Fig. 1B, since materials are selected from a large choice of materials and the dielectrics 2 and the resistive element 3 are formed previously on the metal foil 1, a capacitor and resistor excellent in characteristics may be incorporated in the same layer in a mingled state. Furthermore, since an organic material is used as the insulating board 5, lighter weight may be realized than in the case of ceramics. Furthermore, in order to form a vortical inductor, in advance the conductive paste may be vortically coated on the metal foil 1.

[0089] Fig. 3 is a perspective view showing the double-sided wiring board 7 that can be formed according to the embodiment explained in Fig. 1A and Fig. 1B, or the double-sided wiring board 7a that can be formed according to the embodiment explained in Fig. 2A and Fig. 2B. As shown in Fig. 3, on both sides (one side may be allowed) of the insulating board 5, a resistor due to the resistive element 3, a capacitor due to the dielectrics 2, and a vortical inductor due to the pattern 1a may be incorporated in a state previously provided to the wiring boards 7/7a. By making use of the wiring pattern 1a as a land to mount surface mount components and semiconductor devices on both sides of the double-sided wiring board 7a, it may be of course used as a mounted wiring board as it is.

[0090] Fig. 4A and Fig. 4B are diagrams showing a process carried out to make the double-sided wiring board 7a (7) that is fabricated according to the process shown in Fig. 1A and Fig. 1B, or Fig. 2A and Fig. 2B a material of a four-layered wiring board. Fig. 4A is a sectional view, and Fig. 4B is a perspective view. Fig. 5A and Fig. 5B are diagrams showing a necessary metal foil when a four-layered wiring board is fabricated with the double-sided wiring board 7a (7) fabricated according to the process shown in Fig. 1A and Fig. 1B, or Fig.

2A and Fig. 2B and a process applied thereon. Fig. 5A is a sectional view, and Fig. 5B is a perspective view. Furthermore, already explained regions in these figures are given the same reference numerals. An N-layered wiring board is a wiring board in which the number of the wiring layers is N.

[0091] First, as shown in Fig. 4A and Fig. 4B, in order to use the double-sided wiring board 7a (7) as a core wiring board, conductive bumps 9 are formed on necessary positions on one side thereof (positions according to a layout as a particular four-layered wiring board). The formation of the conductive bumps 9 may be implemented substantially similarly to the already mentioned formation of the conductive bump 8. Thereby, a wiring board material 71 having the conductive bumps 9 is formed.

[0092] At the same time, as shown in Fig. 5A and Fig. 5B, a metal foil 1 to be the third wiring layer is prepared, and at necessary positions on the single side thereof (positions according to a layout as a particular four-layered wiring board) the conductive bumps 9 are formed. The formation of the conductive bumps 9 is performed also similarly to the above. Thereby, a metal foil 11 having the conductive bumps 9 is formed.

**[0093]** Fig. 6 includes diagrams showing a process for fabricating a four-layered wiring board by use of the wiring board material 71 fabricated by the process shown in Fig. 4A and Fig. 4B and the metal foil 11 shown in Fig. 5A and Fig. 5B as materials. Fig. 7 includes perspective views showing the process shown in Fig. 6. In Fig. 6 and Fig. 7, the already explained regions are given the same reference numerals.

[0094] As shown in Fig. 6 upper side and Fig. 7 upper side, respectively, first, the metal foil 1 is disposed through a prepreg to be an insulating board 51 so as to face a surface on which the conductive bumps 9 are formed of the wiring board material 71, and a side on which the conductive bumps 9 are formed of the metal foil 11 is disposed through the prepreg to be the insulating board 51 so as to face a surface on which a conductive bump 9 is not formed of the wiring board material 71. The prepreg to be the insulating board 51 may be one similar to the above-mentioned prepreg to be the insulating board 5.

[0095] Next, as shown in Fig. 6 center and Fig. 7 center, a four-layered wiring board 21 is obtained by stacking, pressurizing and heating five, that is, the metal foil 1, insulating board 51, wiring board material 71, insulating board 51, and metal foil 11, and thereby integrating these. In the double-sided wiring board 21, each of the wiring patterns 1a on both sides of the wiring board material 71 is integrated so as to sink in a thickness direction of the insulating boards 51, and the conductive bumps 9 penetrate through the each of the insulating boards 51 and come into an electrical contact with the opposing metal foil 1 or the pattern 1a. Such a state is realized because the insulating boards 51 had thermoplasticity and thermo-setting properties, and the con-

ductive bumps 9 are originally formed in substantial

[0096] In the four-layered wiring board 21, since an electrical continuity between an outer wiring layer and an inner wiring layer is established by means of the conductive bumps 9, there is no need of performing a further process such as through-hole formation for establishing an electrical continuity between these. Accordingly, since a space for use in through-hole formation is not necessary, a higher density four-layered wiring board may be obtained. In addition, in view of not adversely affecting on the layout of the other layers, needlessness of the through-hole formation is more significant as the number of wiring layers increase.

[0097] Next, as shown in Fig. 6 lower side and Fig. 7 lower side, the metal foils 1 on both sides of the four-layered wiring board 21 are patterned into a pattern 1b necessary as a wiring board. Due to the patterning, a four-layered wiring board 22 is formed. In the patterning, as mentioned above, existing methods may be used, and due to the patterning a vortically shaped inductor may be formed.

[0098] Furthermore, although the processes following the above are not shown by means of the drawings, the formation of solder resist and plating layers including on the pattern 1b, mounting of surface-mounting components on the pattern 1b, or flip-chip mounting of semiconductor chips may be implemented according to existing methods.

[0099] In the above-explained embodiments, an explanation is given for a case where a four-layered wiring board is fabricated with the double-sided wiring board 7a (7) obtained according to the fabricating method that is explained in Fig. 1A and Fig. 1B, or Fig. 2A and Fig. 2B as a core wiring board. Accordingly, the four-layered wiring board may be fabricated while maintaining features as the already-explained double-sided wiring board 7a (7). In addition, since the insulating board 51 that is an organic material is used when forming into a multi-layered structure, the formed multi-layered wiring board may be made lighter than ceramic one.

[0100] In the above explanation, a four-layered wiring board is fabricated by use of the double-sided wiring board 7a (7). A three-layered wiring board may be substantially similarly fabricated. That is, as one method, in Fig. 6 upper side, when three from the top (three of metal foil 1, insulating board 51 and wiring board material 71) is stacked, pressurized and heated and thereby these are integrated, a three-layered wiring board is obtained. Furthermore, as another method, in Fig. 6 upper side one, by stacking, pressurizing and heating three from the bottom (since in this case, the conductive bump 9 on the wiring board material 71 is unnecessary, the three is the wiring board material 7a (7), insulating board 51 and metal foil 11), and thereby integrating these, a three-layered wiring board is obtained.

[0101] Even in such a three-layered wiring board, a three-layered wiring board may be realized while main-

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taining features as the above-explained double-sided wiring board 7a (7).

[0102] Furthermore, in the above explanation, cases where passive elements are not previously incorporated in the third and fourth wiring layers of the four-layered wiring board and in the third wiring layer of the three-layered wiring board are explained. However, in Fig. 6 upper side one, by use of the coated/formed metal foil 4 (the formation surface of the passive element is used directed downward) shown in Fig. 1A or Fig. 2A in place of the upper side metal foil 1, and by use of the conductive bump formed metal foil 4a shown in Fig. 2A in place of the metal foil 11, passive elements may be incorporated in the third and fourth wiring layers.

[0103] According to these, the four-layered wiring board 22 may be formed in the shape where the third and fourth wiring layers of the four-layered wiring board 22 are previously provided with the resistor due to the resistive element 3 and the capacitor due to the dielectrics 2. Since the resistors and capacitors with which the third and fourth wiring layers are provided are also previously formed on the metal foil 1 before the stacking, there are the advantages similar to the resistor and the capacitor with which the first and second wiring layers are provided. Furthermore, the resistors with which the third and fourth wiring layers are provided may be also trimmed by use of the pattern 1b. In addition, by previously coating a vortical conductive paste on the metal foil 1, the inductor due to the conductive paste may be formed on the third and fourth wiring layers.

**[0104]** Furthermore, when the above-explained method is repeated and used, a wiring board having wiring layers exceeding four layers may be easily formed. When, for instance, a six-layered wiring board is fabricated, in Fig. 6 upper side one, in place of the wiring board material 71, one in which the conductive bumps are formed on a single side of the flour-layered wiring board 22 may be utilized. According to such repetition, furthermore multi-layered wiring boards are obtained.

[0105] Fig. 8 is a perspective view showing an example of the four-layered wiring board fabricated according to the fabricating method shown in Fig. 6 and Fig. 7. In the four-layered wiring board 22a in this example, by use of the pattern 1b of the outer wiring layer, a land for mounting a semiconductor device 32 and surfacemount components is formed, and a loop antenna 31 is formed near an outer periphery of the four-layered wiring board 22a.

[0106] Thereby, the semiconductor device 32, the loop antenna 31 and the passive elements (ones that are incorporated in the wiring board and surface-mounted components) necessary for, for example, an IC card (integrated circuit card) that delivers information via radio are integrated and formed into a four-layered wiring board. The formation of the loop antenna 31 by use of such the pattern may be performed by use of the pattern 1a on the double-sided wiring board 7 (7a) already described in Fig. 1B or Fig. 2B.

**[0107]** Fig. 9 is a partial sectional view as an example of the double-sided wiring board fabricated according to the fabricating method according to still another embodiment of the present invention. Constituent elements that are already explained are given the same reference numerals.

[0108] This double-sided wiring board 7b is different from one shown in Fig. 2B in that as a lead wire of the resistive element 3, a conductive bump 8 that penetrates through the insulating board 5 is in direct use. In order to fabricate a double-sided wiring board in such a configuration, when the metal foil 4a shown in Fig. 2A is formed, the position of the conductive bump 8 need only be set so that it may be formed on the resistive element 3 of the metal foil 1.

**[0109]** Then, as shown in Fig. 2B, these are laminated and followed by patterning the metal foils 1 on both sides. In the patterning, the metal foil 1 on a side in contact with the resistive element 3 is patterned so that the metal foil 1 may not completely come into contact with the resistive element 3.

[0110] In thus configured resistor, since a lead wire thereof is not a metal used in the metal foil 1, without considering compatibility with the metal a resistive paste to be the resistive element 3 may be selected. The compatibility shows difficulty with which chemical and physical changes occurs at interfaces of, for instance, the metal (for instance, copper) of the metal foil 1 and the resistive element 3 when these come into contact. Bad compatibility may cause earlier corrosion on any one of these. In the present embodiment, since it is not necessary to consider the compatibility at least with the metal foil 1, a range of choice of the resistive pastes may be further expanded. Accordingly, further higher precision may be accomplished.

**[0111]** Fig. 10 is a bottom view as an example of the double-sided wiring board 7b shown in Fig. 9. The regions corresponding to Fig. 9 are given the same reference numerals.

[0112] As shown in Fig. 10, the contact between the resistive element 3 and the conductive bump 8 may occur at a plurality of points (three in this case shown in the figure) at one end. This is because while a shape of the resistive element 3 is varied in length and breadth according to a necessary resistance value, the size of the conductive bump 8 is normally fixed due to the simultaneous formation by use of, for instance, printing. By use of a plurality number of the conductive bumps 8, the lead wires may be drawn out corresponding to the size of the resistive element 3.

**[0113]** Fig. 11 is a partial sectional view showing another example to one example shown in Fig. 9. The constituent elements that are already explained are given the same reference numerals.

**[0114]** The double-sided wiring board 7c is similar to one shown in Fig. 9 in that the conductive bumps 8a that penetrate through the insulating board 5 is directly formed on the resistive element 3. However, in the case

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shown in Fig. 11, the conductive bumps 8a are used, not as the lead wire, as heat conductor to the resistive element 3. The conductive bump 8a works as a heat conductive bridge with the wiring pattern 1c on a rear surface side of the resistive element 3. One resistive element 3 may be provided with a plurality of the conductive bumps 8a.

[0115] In a resistor that is configured so as to have the conductive bumps 8a for heat conduction, Joule heat that is generated due to the resistor may be efficiently dissipated from both surfaces of the wiring board by use of the conductive bumps 8a and the wiring pattern 1c as heat-sink. Accordingly, since the resistor is increased in its power rating, thereby a degree of freedom in circuit designing applied for the wiring board may be advantageously improved.

**[0116]** Fig. 12A and Fig. 12B are partial sectional views for explaining one example of a double-sided wiring board fabricated according to the fabricating method according to still another embodiment of the present invention. Fig. 12A shows an intermediate stage to a state shown in Fig. 12B. Furthermore, the constituent elements that are already explained are provided with the same reference numerals.

**[0117]** The double-sided wiring board 7d is different from one shown in Fig. 1A and Fig. 1B in that the pattern 1a and an electrical conductor 35 formed from the conductive paste are used as both end electrodes of the dielectrics 2.

[0118] In order to fabricate a double-sided wiring board in such a configuration, first, as shown in Fig. 12A, after dielectrics 2 is coated/formed on a metal foil 1, a conductive paste to be an electrical conductor 35 is coated including on the dielectrics 2 and extending onto the metal foil 1. In the coating, a method identical to that used in the coating of the dielectric paste to be the dielectrics 2 may be utilized. Treatment such as predetermined drying and so on is applied to the coated conductive paste. Then, the metal foil 1 is used in place of the coated/formed metal foil 4 shown in Fig. 1B upper side or Fig. 2B upper side and laminated. By further patterning the metal foils 1 on both sides, the double-sided wiring board 7d as shown in Fig. 12B may be obtained (in a strict sense, since there are the conductive bumps 8 in Fig. 12B, it shows a case applied to the case shown in Fig. 2B. However, the conductive bump 8 is not indispensable).

**[0119]** In a structure around the dielectrics 2 like this, since the pattern 1a and the electrical conductor 35 sandwich the dielectrics 2 and form a so-called parallel plate capacitor, a capacitor having higher capacitance may be formed. Furthermore, all of the already explained improvement effect as the passive element and wiring board is maintained.

**[0120]** Fig. 13A and Fig. 13B are partial sectional views for explaining another example to one example shown in Fig. 12A and Fig. 12B. Fig. 13A shows an intermediate stage to a state shown in Fig. 13B. Further-

more, the constituent elements that are already explained are provided with the same reference numerals. [0121] The double-sided wiring board 7e is one in which the aforementioned parallel plate capacitor structure is further actively formed. Due to the lamination like this, a capacitor having higher capacitance may be formed.

[0122] Specifically, as shown in Fig. 13A, first, dielectrics 26 is coated/formed on a metal foil 1 followed by coating a conductive paste to be an electrical conductor 36 so as to include on the dielectrics 26 and extend onto the metal foil 1. After the coating, processes such as predetermined drying and so on are performed. Next, a dielectric paste to be the dielectrics 27 is coated so as to include on the electrical conductor 36 and come into contact with the dielectrics 26. After the coating, processes such as predetermined drying and so on are performed. Next, the conductive paste to be an electrical conductor 38 is coated so as to include on the dielectrics 27, not to come into contact with the electrical conductor 36, and to extend onto the metal foil 1. After the coating, processes such as predetermined drying and so on are performed.

[0123] Furthermore, the dielectric paste to be dielectrics 28 is coated so as to include on the electrical conductor 38 and come into contact with the dielectric 27. After the coating, processes such as predetermined drying and so on are performed. Next, a conductive paste to be an electrical conductor 37 is coated so as to include on the dielectrics 28, not to come into contact with the electrical conductor 38, and to come into contact with the electrical conductor 36. After the coating, processes such as predetermined drying and so on are performed. The coating of the dielectric paste to be individual dielectrics 26, 27 and 28, and the coating of the conductive paste to be individual electrical conductors 36, 37 and 38 are performed similarly to the cases of the dielectrics 2 and the electrical conductor 35 in the embodiment shown in, for instance, Fig. 12A and Fig. 12B. [0124] Then, the metal foil 1 is used in place of the coated/formed metal foil 4 shown in Fig. 1B upper side or Fig. 2B upper side and is laminated. Furthermore, by patterning the metal foils 1 on both sides, a double-sided wiring board 7e as shown in Fig. 13B may be obtained (since there are the conductive bumps 8 in Fig. 13B, in a strict sense, it shows a case applied to the case shown in Fig. 2B. However, the conductive bumps 8 are not indispensable). The patterning of the metal foil 1 is performed so that as one electrode a pattern that occupies almost on the dielectrics 26 and comes into contact also with the electrical conductor 38 may exist, and as another electrode a pattern having an electrical continuity with electrical conductors 36 and 37 may exist.

**[0125]** A capacitor due to such lamination may enable to realize a further higher capacitance by further performing similar lamination. Furthermore, all of the aforementioned improvement effect as the passive element and the wiring board is maintained.

[0126] Although the above-explained examples due to Figs. 9 through 13B are of the cases of the double-sided wiring board, it is obvious that outer wiring layers in the four-layered wiring boards (or the above-explained three-layered wiring boards) as shown in Fig. 6 and Fig. 7 may allow to form the above-explained passive elements. Furthermore, the situations are identical also in the case of a multi-layered, exceeding four layers, wiring board.

**[0127]** Fig. 15A and Fig. 15B are diagrams for explaining one example of a four-layered wiring board fabricated according to the fabricating method according to still another embodiment of the present invention. Fig. 15A is a sectional view and Fig. 15B is a top view thereof. The aforementioned constituent numerals are given the same reference numerals.

[0128] The four-layered wiring board is different from one shown in Fig. 6 and Fig. 7 in that there are formed magnetically permeable bumps 8A and 9A that, respectively, penetrate through insulating boards 5 and 51 and these magnetically permeable bumps 8A and 9A are in contact in a penetrating direction. Furthermore, patterns 1a and 1b are patterned, respectively, as shown in Fig. 15B, so as to surround the magnetically permeable bumps 8A and 9A and, as shown in Fig. 15A, the conductive bumps 8 and 9 bring ambient patterns into an electrical continuity in a vertical direction.

[0129] That is, the magnetically permeable bumps 8A and 9A work as a core of an inductor, and each patterns 1a and 1b work as a helical inductor coil as a whole. In thus structured inductor, since the magnetically permeable material is used as a core and a coil is realized as a helical coil around the core, an inductance value may be increased. It is obvious that the inductor due to such a core and helical structure is, without restricting to such the four-layered wiring board, may be configured similarly even in a double-sided wiring board, three-layered wiring board and multi-layered, exceeding four layers, wiring board.

**[0130]** In order to fabricate such the inductor that is incorporated in a four-layered wiring board, first, when a double-sided wiring board as a core wiring board is fabricated, in place of the coated/formed metal foil 4 in Fig. 2B upper side, a magnetically permeable bump formed metal foil fabricated according to the similar knack as the conductive bump formed metal foil 4a is used.

**[0131]** A magnetically permeable bump 8A may be formed on a place necessary as a wiring board on the coated/formed metal foil 4 by means of, for instance, screen printing. For this, as a magnetically permeable paste, for instance, one in which magnetically permeable material powder (for instance, ferrite powder) is dispersed in a paste-like resin followed by mingling a volatile solvent is prepared, and this is coated by means of screen-printing on the metal foil 4. The magnetically permeable bump 8A is necessary to have a height enough to penetrate through the insulating board 5. Accordingly,

the magnetically permeable bump 8A is formed to have a substantially conical shape as a whole.

**[0132]** Then, following the above, processes up to one shown in Fig. 2B lower side are implemented. According to the processes up to this one, first, in the double-sided wiring board, an inductor due to a helical structure may be obtained.

[0133] Furthermore, in fabricating in a four-layered wiring board, in place of the metal foil 1 in Fig. 6 upper side, a metal foil provided with the magnetically permeable bump 9A thereon is used (a surface on which the magnetically permeable bump 9A is formed is directed downward). In addition, in place of the wiring board material 71 in Fig. 6 upper side, one in which the conductive bump 9 is formed on one side (top surface in the figure) of the double-sided wiring board including the aforementioned magnetically permeable bump 8A, and the magnetically permeable bump 9A is formed on the other surface is used. The magnetically permeable bump 9A can be formed similarly to the above.

[0134] Thereafter, the processes up to one shown in Fig. 6B lower side are performed. Thereby, an inductor due to a helical structure in which all layers of a four-layered wiring layer are used as coil can be obtained. Furthermore, by performing similarly, an inductor due to a helical structure in which all layers of an N-layered wiring layer are used as coil can be obtained.

[0135] Fig. 16A and Fig. 16B are diagrams for explaining another example to one example shown in Fig. 15A and Fig. 15B. Fig. 16A is a sectional view thereof and Fig. 16B is a top view thereof. The aforementioned constituent elements are given the same reference numerals

**[0136]** This four-layered wiring board is different from one shown in Fig. 15A and Fig. 15B in that a magnetically permeable pillared body 82 that penetrates through the insulating boards 5 and 51 is used in place of the magnetically permeable bumps 8A and 9A of the four-layered wiring board shown in Fig. 15A and Fig. 15B.

[0137] In this case too, the magnetically permeable pillared body 82 works as a core of an inductor, and each patterns 1a and 1b work as a helical inductor coil as a whole. Accordingly, similarly to the above, an inductance value may be increased. It is obvious that an inductor due to such a core of the magnetically permeable pillared body 82 and a helical structure, without restricting to such a four-layered wiring board, may be configured similarly even in a double-sided wiring board, three-layered wiring board, and multi-layered, exceeding four layers, wiring board.

[0138] In order to fabricate such an inductor incorporated in four-layered wiring board, a four-layered wiring board that has undergone the process shown in Fig. 6 lower side may be provided with a through-hole 81, and the formed through-hole 81 may be filled in with a magnetically permeable material. Similarly, a multi-layered, exceeding four layers, wiring board also, after a multi-

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layered wiring board having finally needed layers has been formed, may be provided with a through-hole, and the formed through-hole may be filled in with a magnetically permeable material. As a magnetically permeable material as mentioned above may be used, or previously solidified magnetically permeable pillared body may be inserted and fixed.

**[0139]** The present invention has been described with reference to certain preferred embodiments, but it will be understood that variations and modifications can be made within the spirit and scope of the invention.

#### Claims

 A method for fabricating a wiring board provided with a passive element, comprising:

coating a resistive paste and/or a dielectric 20 paste on at least any one of first surfaces of a first metal foil and a second metal foil each of which has the first surface and a second surface:

arranging an insulating board having thermoplasticity and thermo-setting properties so as to face the first surface of the first metal foil, and arranging the first surface side of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board;

forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil to integrate these; and patterning the first metal foil and/or the second metal foil of the formed double-sided wiring board.

2. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

forming a substantially conical conductive bump on the first surface of the first metal foil;

wherein the forming a double-sided wiring board is performed so that the formed conductive bump penetrates through the insulating board and establishes an electrical contact with the second metal foil.

**3.** A method for fabricating a wiring board provided with a passive element as set forth in claim 1:

wherein the patterning the first metal foil and/ or the second metal foil includes formation of an inductor that is vortically formed due to a pattern and/ or a loop antenna that is formed loop-like due to a pattern.

4. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

trimming a resistor formed from the resistive paste by use of the patterned first metal foil and/ or the patterned second metal foil as an electrode.

5. A method for fabricating a wiring board provided with a passive element as set forth in claim 1:

wherein the coating the resistive paste and/or the dielectric paste includes removing a periphery portion thereof after the coating.

6. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

> forming a substantially conical conductive bump on a first surface of a third metal foil having the first surface and a second surface; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, and arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface that faces the third metal foil of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged third metal foil, second insulating board, and double-sided wiring board to integrate these so that the conductive bump formed on the third metal foil penetrates through the second insulating board and establishes an electrical contact with the first metal foil; and patterning the third metal foil of the formed three-layered wiring board.

7. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

coating a resistive paste and/or a dielectric paste on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical conductive bump on the first surface of the third metal foil; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, and arranging a first metal foil side of the double-sided wiring board so as to face a surface different from a surface that faces the third metal foil of the second insulating board;

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forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged third metal foil, second insulating board, and double-sided wiring board to integrate these so that the conductive bump formed on the third metal foil penetrates through the second insulating board and establishes an electrical contact with the first metal foil; and patterning the third metal foil of the formed three-layered wiring board.

8. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

forming a substantially conical conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the conductive bump of the double-sided wiring board is formed, and arranging a third metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the second insulating board;

forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the arranged double-sided wiring board, second insulating board, and third metal foil to integrate these so that the conductive bump formed on the double-sided wiring board penetrates through the second insulating board and establishes an electrical contact with the third metal foil: and

patterning the third metal foil of the formed three-layered wiring board.

9. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

coating a resistive paste and/or a dielectric paste on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face a side on which the conductive bump of the double-sided wiring board is formed, and arranging the first surface side of the third metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the second insulating board; forming a three-layered wiring board by stacking, pressurizing and heating three, that is, the

arranged double-sided wiring board, second insulating board, and third metal foil to integrate these so that the conductive bump formed on the double-sided wiring board penetrates through the second insulating board and establishes an electrical contact with the third metal foil: and

patterning the third metal foil of the formed three-layered wiring board.

**10.** A method for fabricating a wiring board provided with a passive element as set forth in any one of claim 6, 7, 8, or 9:

wherein the patterning the third metal foil includes formation of an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern.

**11.** A method for fabricating a wiring board provided with a passive element as set forth in claim 7 or 9:

wherein the coating a resistive paste and/or a dielectric paste on the first surface of the third metal foil includes removing a periphery portion thereof after the coating.

**12.** A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

forming a substantially conical conductive bump on a first surface of a third metal foil having the first surface and a second surface;

forming a substantially conical second conductive bump on the second surface of the second metal foil of the formed double-sided wiring board:

arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermoplasticity and thermosetting properties so as to face a side on which the second conductive bump is formed of the double-sided wiring board, and arranging a fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board;

forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil to integrate these so that the conductive bump formed on the third metal foil penetrates through the second insu-

lating board and establishes an electrical contact with the first metal foil and the second conductive bump formed on the double-sided wiring board penetrates through the third insulating board and establishes an electrical contact with the fourth metal foil; and patterning the third metal foil and/or the fourth metal foil of the formed four-layered wiring board.

13. A method for fabricating a wiring board provided with a passive element as set forth in claim 1, further comprising:

coating a resistive paste and/or a dielectric paste on at least any one or first surfaces of a third and fourth metal foils each of which has the first surface and a second surface;

forming a substantially conical conductive bump on the first surface of the third metal foil; forming a substantially conical second conductive bump on the second surface of the second metal foil of the formed double-sided wiring board;

arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermoplasticity and thermosetting properties so as to face a side on which the second conductive bump is formed of the double-sided wiring board, and arranging the first surface side of the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board; forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil to integrate these so that the conductive bump formed on the third metal foil penetrates through the second insulating board and establishes an electrical contact with the first metal foil and the second conductive bump formed on the double-sided wiring board penetrates through the third insulating board and establishes an electrical contact with the fourth metal foil; and patterning the third metal foil and/or the fourth metal foil of the formed four layered wiring

**14.** A method for fabricating a wiring board provided with a passive element as set forth in claim 12 or 13:

board.

wherein the patterning the third metal foil and/ or the fourth metal foil includes formation of an inductor that is vortically formed due to a pattern and/ or a loop antenna that is formed loop-like due to a pattern.

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15. A method for fabricating a wiring board provided with a passive element as set forth in claim 13:

wherein the coating a resistive paste and/or a dielectric paste on at least any one of the first surfaces of the third and fourth metal foils includes removing a periphery portion thereof after the coating.

16. A method for fabricating a wiring board provided with a passive element, comprising:

coating a resistive paste on a first surface of at least a first metal foil of the first metal foil and a second metal foil each of which has a first surface and a second surface:

forming a substantially conical conductive bump on a resistive element formed of the coated resistive paste;

arranging an insulating board having thermoplasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board;

forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil to integrate these so that the formed conductive bump penetrates through the insulating board and establishes an electrical contact and/or a heat conductive contact with the second metal foil; and

patterning the first metal foil and the second metal foil of the formed double-sided wiring board.

17. A method for fabricating a wiring board provided with a passive element, comprising:

> coating a dielectric paste on a first surface of at least a second metal foil of a first metal foil and the second metal foil each of which has a first surface and a second surface:

> coating a conductive paste so as to include on the coated dielectric paste and extend onto the first surface on which the dielectric paste is coated:

> arranging an insulating board having thermoplasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a sur-

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face to which the first metal foil faces of the insulating board;

forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil to integrate these; and patterning at least the second metal foil of the formed double-sided wiring board.

**18.** A method for fabricating a wiring board provided with a passive element, comprising:

coating a dielectric paste on a first surface of at least a second metal foil of a first metal foil and the second metal foil each of which has a first surface and a second surface;

coating a first conductive paste so as to include on the coated dielectric paste and extend onto the first surface on which the dielectric paste is coated:

coating a second dielectric paste so as to include on the coated first conductive paste; coating a second conductive paste so as to include on the coated second dielectric paste, to extend onto the first surface on which the second dielectric paste is coated, and not to come into contact with the first conductive paste; arranging an insulating board having thermoplasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board;

forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil to integrate these; and patterning at least the second metal foil of the formed double-sided wiring board.

**19.** A method for fabricating a wiring board provided with a passive element, comprising:

forming a substantially conical conductive bump on a first surface of a first metal foil having the first surface and a second surface; forming a substantially conical magnetically permeable bump on a first surface of a second metal foil having the first surface and a second surface:

arranging an insulating board having thermoplasticity and thermosetting properties so as to face the first surface of the first metal foil, and arranging the first surface side of the second metal foil so as to face a surface different from a surface to which the first metal foil faces of the insulating board; forming a double-sided wiring board by stacking, pressurizing and heating three, that is, the arranged first metal foil, insulating board, and second metal foil to integrate these so that the formed conductive bump and magnetically permeable bump penetrate through the insulating board and establish a contact with the first/second metal foil; and

patterning the first metal foil and the second metal foil of the formed double-sided wiring board

**20.** A method for fabricating a wiring board provided with a passive element as set forth in claim 19, further comprising:

forming a substantially conical second conductive bump on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical second magnetically permeable bump on a first surface of a fourth metal foil having the first surface and a second surface;

forming a substantially conical third conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; forming a substantially conical third magnetically permeable bump on a surface on the first metal foil side of the formed double-sided wiring board;

arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging a first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermoplasticity and thermosetting properties so as to face a side on which the third conductive bump is formed of the double-sided wiring board, and arranging the first surface side of the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating board;

forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil to integrate these so that the second conductive bump formed on the third metal foil penetrates through the second insulating board and establishes an electrical contact with the first metal foil, the second magnetically permeable bump formed on the double-sided wiring board penetrates through the second insulating board and establishes a contact with the third metal foil, the third con-

ductive bump formed on the double-sided wiring board penetrates through the third insulating board and establishes an electrical contact with the fourth metal foil, and the third magnetically permeable bump formed on the fourth metal foil penetrates through the third insulating board and establishes a contact with a surface on a side of the second metal foil of the double-sided wiring board; and patterning the third metal foil and the fourth metal foil of the formed four-layered wiring

**21.** A method for fabricating a wiring board provided with a passive element as set forth in claim 2, further comprising:

board.

forming a through-hole in the formed doublesided wiring board; and filling a magnetically permeable material in the formed through-hole.

22. A method for fabricating a wiring board provided with a passive element as set forth in claim 1 further comprising forming a substantially conical conductive bump on the first surface of the first metal foil, wherein the forming a double-sided wiring board is performed so that the formed conductive bump penetrates through the insulating board and establishes an electrical contact with the second metal foil, the method further comprising:

forming a substantially conical second conductive bump on a first surface of a third metal foil having the first surface and a second surface; forming a substantially conical third conductive bump on the second surface of the second metal foil of the formed double-sided wiring board; arranging a second insulating board having thermo-plasticity and thermosetting properties so as to face the first surface of the third metal foil, arranging the first metal foil side of the double-sided wiring board so as to face a surface different from a surface to which the third metal foil faces of the second insulating board, arranging a third insulating board having thermoplasticity and thermosetting properties so as to face a side on which the third conductive bump is formed of the double-sided wiring board, and arranging the fourth metal foil so as to face a surface different from a surface that faces the double-sided wiring board of the third insulating

forming a four-layered wiring board by stacking, pressurizing and heating five, that is, the arranged third metal foil, second insulating board, double-sided wiring board, third insulating board, and fourth metal foil to integrate these

so that the second conductive bump formed on the third metal foil penetrates through the second insulating board and establishes an electrical contact with the first metal foil, and the third conductive bump formed on the doublesided wiring board penetrates through the third insulating board and establishes an electrical contact with the fourth metal foil;

patterning the third metal foil and the fourth metal foil of the formed four-layered wiring board:

forming a through-hole in the formed four-layered wiring board; and

filling a magnetically permeable material in the formed through-hole.

23. A wiring board provided with a passive element, comprising:

an insulating board having a first surface and a second surface;

a layered resistive element and/or a layered dielectrics disposed on the first surface and/or the second surface of the insulating board so as to sink in a thickness direction of the insulating board; and

a first wiring layer and a second wiring layer that are, respectively, disposed on the first surface and the second surface of the insulating board, and each of which has a connection with the layered resistive element and/or the layered dielectrics disposed on the corresponding first/second surface.

5 24. A wiring board provided with a passive element as set forth in claim 23, further comprising:

a conductive bump that penetrates through the insulating board;

wherein each of the first and second wiring layers has an electrical connection with the conductive bump.

5 25. A wiring board provided with a passive element as set forth in claim 23:

wherein at least one of the first and second wiring layers has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern.

**26.** A wiring board provided with a passive element as set forth in claim 23, further comprising:

a second insulating board disposed in contact with the first wiring layer side of the insulating board;

a conductive bump that penetrates through the

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second insulating board; and a third wiring layer disposed on a side different from the insulating board side of the second insulating board;

wherein the first wiring layer of the insulating board is disposed so as to sink in a thickness direction of the second insulating board; and

each of the first and third wiring layers has an electrical connection with the conductive bump.

**27.** A wiring board provided with a passive element as set forth in claim 26, further comprising:

a second layered resistive element and/or a second layered dielectrics disposed on the third wiring layer side of the second insulating board so as to sink in a thickness direction of the second insulating board;

wherein the third wiring layer has a connection with the second layered resistive element/the second layered dielectrics.

**28.** A wiring board provided with a passive element as set forth in claim 26:

wherein the third wiring layer has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern

**29.** A wiring board provided with a passive element as set forth in claim 26, further comprising:

a third insulating board disposed in contact with the second wiring layer side of the insulating board:

a second conductive bump that penetrates through the third insulating board; and a fourth wiring layer disposed on a side different from the insulating board side of the third insulating board;

wherein the second wiring layer of the insulating board is disposed so as to sink in a thickness direction of the third insulating board; and

each of the second and fourth wiring layers has an electrical connection with the second conductive bump.

**30.** A wiring board provided with a passive element as set forth in claim 29, further comprising:

a second layered resistive element and/or a second layered dielectrics disposed on the fourth wiring layer side of the third insulating board so as to sink in a thickness direction of the third insulating board;

wherein the fourth wiring layer has a connection with the second layered resistive element/the second layered dielectrics.

5 31. A wiring board provided with a passive element as set forth in claim 29:

wherein the fourth wiring layer has an inductor that is vortically formed due to a pattern and/or a loop antenna that is formed loop-like due to a pattern.

**32.** A wiring board provided with a passive element, comprising:

an insulating board having a first surface and a second surface;

a layered resistive element disposed on the second surface of the insulating board so as to sink in a thickness direction of the insulating board:

a first and second wiring layers disposed on the first surface and second surface of the insulating board, respectively; and

a conductive bump that penetrates through the insulating board and is in an electrical connection and/or a heat conductive connection with the layered resistive element and the first wiring layer.

30. 33. A wiring board provided with a passive element, comprising:

an insulating board having a first surface and a second surface;

a layered electrical conductor disposed on the second surface of the insulating board so as to sink in a thickness direction of the insulating board;

a layered dielectrics disposed in contact with a part of a top surface of the layered electrical conductor so as to sink in a thickness direction of the insulating board; and

a wiring layer that is disposed on the second surface of the insulating board and has individual connections with the layered electrical conductor and the layered dielectrics.

**34.** A wiring board provided with a passive element as set forth in claim 33, further comprising:

a second layered dielectrics disposed under a bottom surface of the layered electrical conductor; and

a second electrical conductor that is disposed containing under a bottom surface of the second layered dielectrics and is in connection with the wiring layer.

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**35.** A wiring board provided with a passive element, comprising:

an insulating board having a first surface and a second surface:

a first and second wiring layers, respectively, disposed on the first surface and the second surface of the insulating board;

a conductive bump that penetrates through the insulating board and is in an electrical connection with the first wiring layer and the second wiring layer; and

a magnetically permeable bump that penetrates through the insulating board;

wherein the first wiring layer has a first pattern that surrounds the magnetically permeable bump;

the second wiring layer has a second pattern that surrounds the magnetically permeable bump; and

the first and second patterns are in continuity due to the conductive bump.

**36.** A wiring board provided with a passive element as set forth in claim 35, further comprising:

a second insulating board disposed on the first wiring layer side of the insulating board;

a third insulating board disposed on the second wiring layer side of the insulating board;

a third wiring layer disposed on a surface side different from the insulating board of the second insulating board;

a fourth wiring layer disposed on a surface side different from the insulating board of the third insulating board;

a second conductive bump that penetrates through the second insulating board and is brought into electrical connections with the first wiring layer and the third wiring layer;

a second magnetically permeable bump that penetrates through the second insulating board:

a third conductive bump that penetrates through the third insulating board and is brought into electrical connections with the second wiring layer and the fourth wiring layer; and a third magnetically permeable bump that penetrates through the third insulating board;

wherein the first wiring layer is disposed so as to sink in a thickness direction of the second insulating board:

the second wiring layer is disposed so as to sink in a thickness direction of the third insulating board:

the magnetically permeable bump, the second magnetically permeable bump, and the third magnetically permeable bump are disposed in series:

the third wiring layer has a third pattern that surrounds the second magnetically permeable bump;

the fourth wiring layer has a fourth pattern that surrounds the third magnetically permeable bump; the first and third patterns are in an electrical continuity due to the second conductive bump; and the second and fourth patterns are in an electrical continuity due to the third conductive bump.

**37.** A wiring board provided with a passive element as set forth in claim 36, comprising:

a pillared body that has a magnetically permeable material and penetrates through the insulating board, the second insulating board, and the third insulating board in place of the magnetically permeable bump, the second magnetically permeable bump, and the third magnetically permeable bump.

FIG. 1A

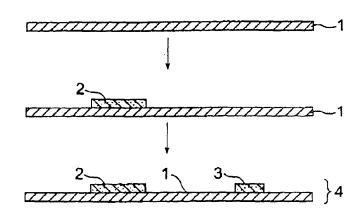


FIG. 1B

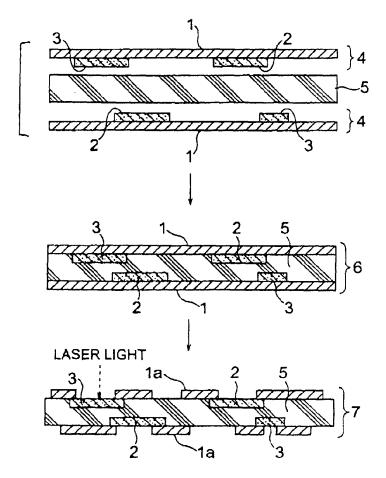


FIG. 2A

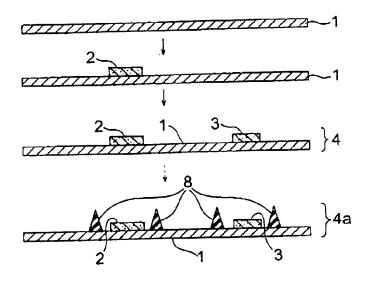


FIG. 2B

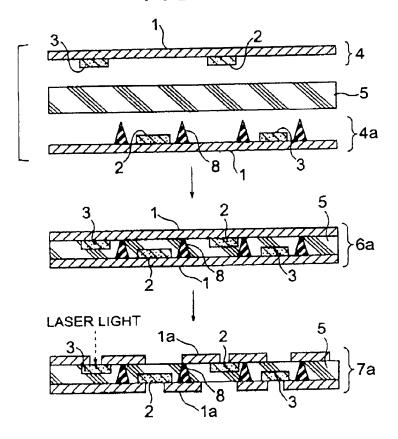


FIG. 3

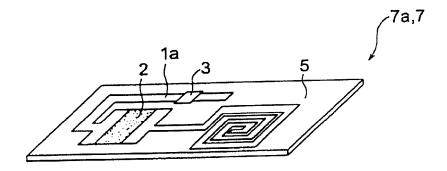
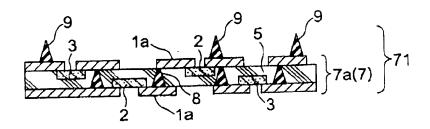


FIG. 4A



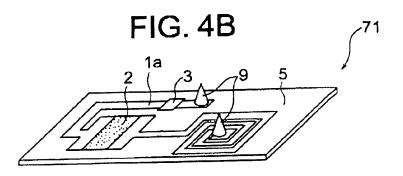
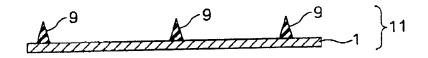


FIG. 5A



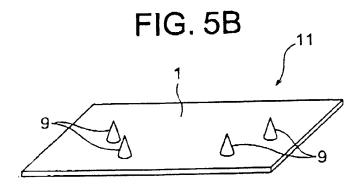


FIG. 6

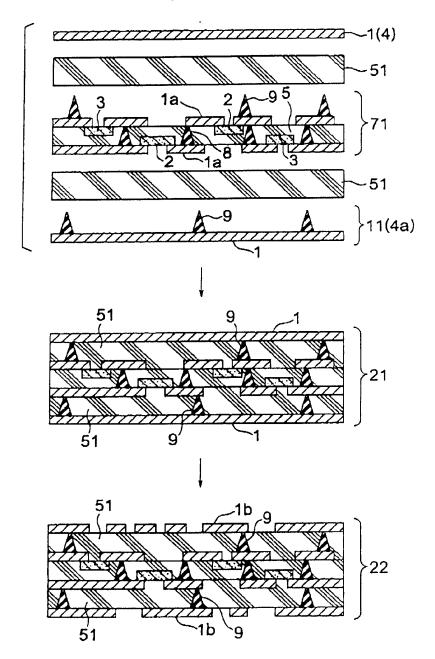


FIG. 7

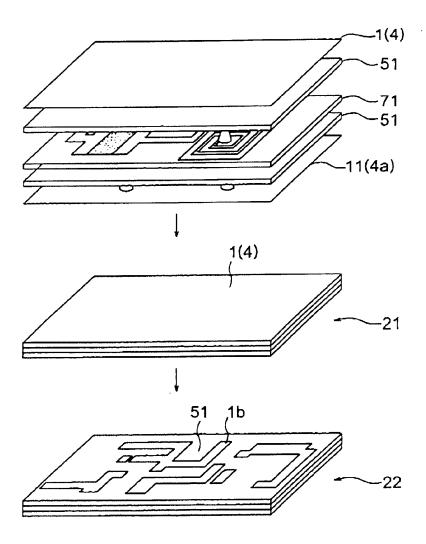


FIG. 8

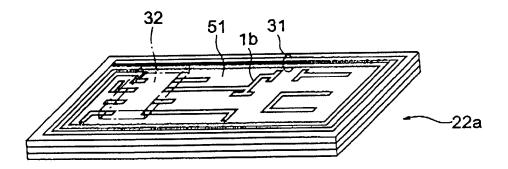


FIG. 9

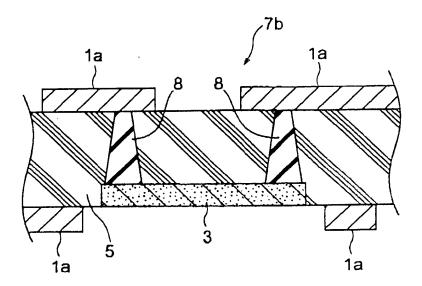


FIG. 10

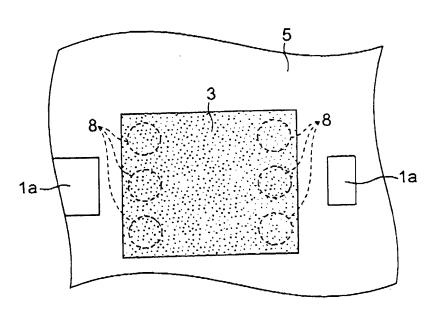


FIG. 11

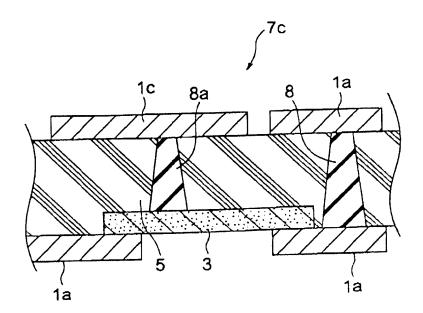
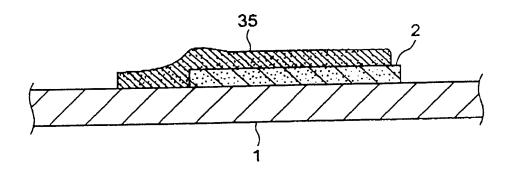


FIG. 12A



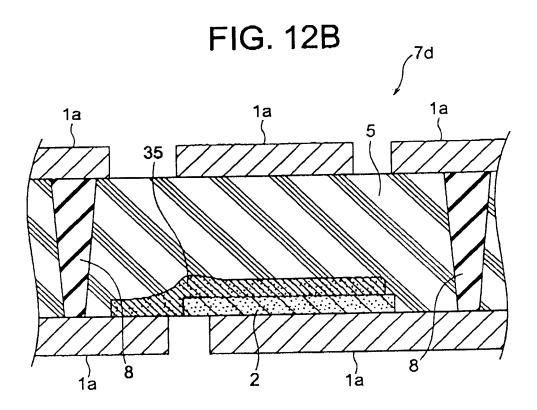
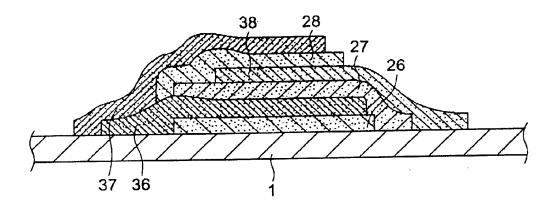


FIG. 13A



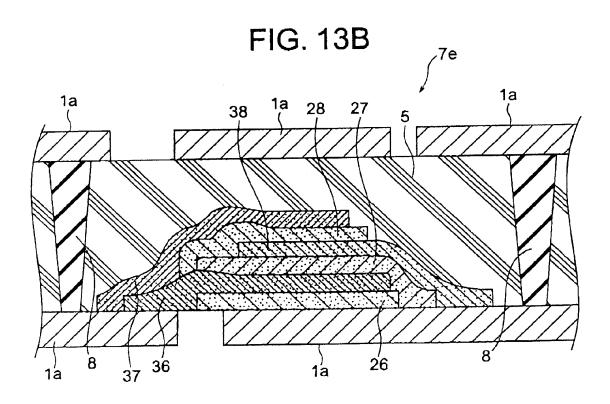


FIG. 14A

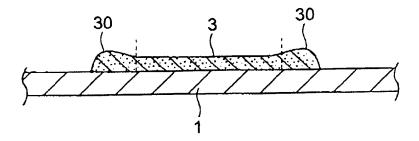


FIG. 14B

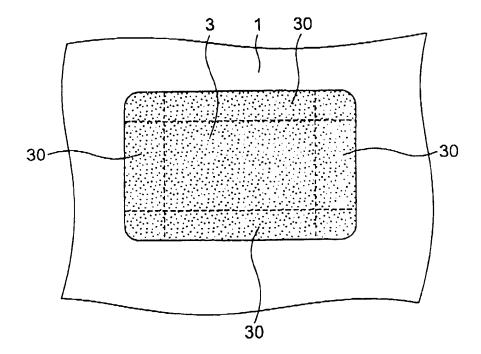


FIG. 15A

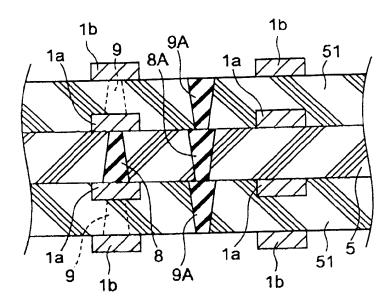


FIG. 15B

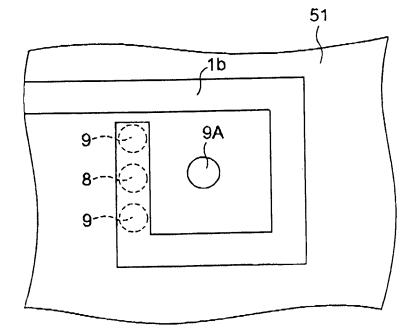


FIG. 16A

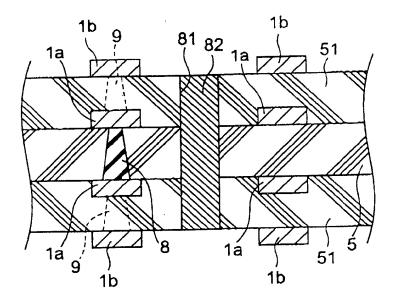
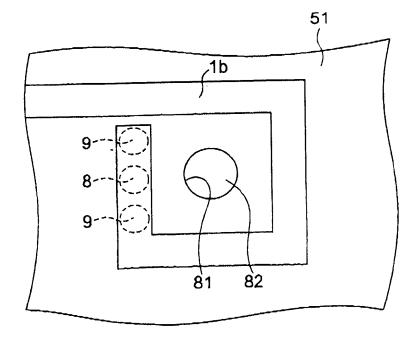


FIG. 16B





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(11) **EP 1 265 466 A3** 

(12)

## **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3: 21.07.2004 Bulletin 2004/30

(51) Int CI.7: **H05K 3/46**, H05K 1/16

(43) Date of publication A2: 11.12.2002 Bulletin 2002/50

(21) Application number: 02253836.7

(22) Date of filing: 31.05.2002

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

Designated Extension States:

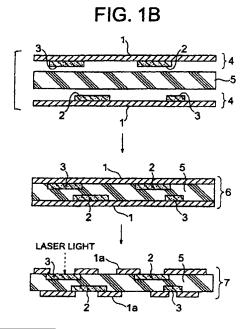
AL LT LV MK RO SI

(30) Priority: **05.06.2001 JP 2001170019 05.06.2001 JP 2001170020** 

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- (74) Representative: Granleese, Rhian Jane
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   57-60 Lincoln's Inn Fields
   London WC2A 3LS (GB)
- (54) Method for fabrication wiring board provided with passive element and wiring board provided with passive element
- (57)A fabricating method of a wiring board (7) provided with passive elements is disclosed. The fabricating method includes coating one or both of resistive paste (3) and dielectric paste (2) on at least any one of first surfaces of a first metal foil and a second metal foil (1) each of which has a first surface and a second surface; arranging an insulating board (5) having thermoplasticity and thermo-setting properties so as to face the first surface of the coated first metal foil (4), and arranging the first surface side of the coated second metal foil (4) so as to face a surface different from a surface to which the coated first metal foil (4) faces of the insulating board (5); forming a double-sided wiring board (6) by stacking, pressurizing and heating the arranged coated first metal foil (4), insulating board (5), and coated second metal foil (4), and thereby integrating these; and patterning the first metal foil and/or the second metal foil (1).





## **EUROPEAN SEARCH REPORT**

Application Number

EP 02 25 3836

|   | DOCUMENTS CONSID   | ERED TO BE F                                  | RELEVANT   | · <sub>T</sub> . · · · · · · · · · ·       |  |  |  |
|---|--|---|--|--|--|--|--|
| Category  | Citation of document with indication, where appro<br>of relevant passages  |   | opriate,   | Relevant<br>to claim                       | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |  |  |
| Х   | US 4 204 187 A (KAK<br>20 May 1980 (1980-0<br>* column 4, line 15  | 5-20)   |  | 1,23                                       | H05K3/46<br>H05K1/16                         |  |  |
| Y   | figures *  |   |  | 2-4,<br>6-10,<br>12-14,<br>17,<br>24-31,33 |  |  |  |
| Y   | PATENT ABSTRACTS OF<br>vol. 1996, no. 11,<br>29 November 1996 (1<br>-& JP 08 195561 A (<br>30 July 1996 (1996-<br>* abstract; figures  | 996-11-29)<br>TOSHIBA CORP<br>07-30)          | ),   | 2,6-10,<br>12-14,<br>24,26-31              |  |  |  |
| Y   | US 5 920 454 A (NOM<br>6 July 1999 (1999-0   |   |  | 3,10,14,<br>17,25,<br>28,31,33             |  |  |  |
|   | * abstract; claim 4  | ; figure 1 *                                  |  | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,    | TECHNICAL FIELDS<br>SEARCHED (Int.CI.7)      |  |  |
| Y   | US 4 870 746 A (KLA<br>3 October 1989 (198<br>* column 6, line 10  | 9-10-03)                                      | figure 4 *   | 4  | H05K<br>H01F                                 |  |  |
| A   | PATENT ABSTRACTS OF<br>vol. 014, no. 359 (<br>3 August 1990 (1990<br>-& JP 02 125692 A (<br>14 May 1990 (1990-0<br>* abstract; figures | E-0959),<br>-08-03)<br>IBIDEN CO LT[<br>5-14) | )),  | 1,23,26                                    |  |  |  |
| Y   | * abstract, rigures  |   | -/   | 7,9,13,<br>14,27,30                        |  |  |  |
|   | The ground as set was six  |   | olaina   |  |  |  |  |
|   | The present search report has  | · · · · · · · · · · · · · · · · · · ·         | claims   | <del></del>                                | Examiner                                     |  |  |
|   | The Hague  | 3 May   |  | Mes  |  |  |  |
| CATEGORY OF CITED DOCUMENTS  X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document |  |   | T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filling date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document |  |  |  |  |

EPO FORM 1503 03.82 (P04C01)



# **EUROPEAN SEARCH REPORT**

Application Number

EP 02 25 3836

|   | DOCUMENTS CONSID  |  |   | Relevant                                |  |
|---|---|--|---|---|--|
| Category  |   | lation of document with indication, where appropri<br>of relevant passages |   |   | CLASSIFICATION OF THE APPLICATION (Int.CI.7) |
| X   | EP 0 073 904 A (ELE<br>WERKE JAKOB PREH)<br>16 March 1983 (1983<br>* page 13, line 12<br>* page 16, line 1 -<br>* figure 2 *          | 1,23   |   |   |  |
| A   | EP 0 409 668 A (OMR<br>23 January 1991 (19<br>* claims; figures *   | 91-01-23)  | ON)   | 1,17                                    |  |
| Х   | · craims, rigures ·   |  |   | 23,33                                   |  |
| Α   | PATENT ABSTRACTS OF<br>vol. 1999, no. 04,<br>30 April 1999 (1999<br>-& JP 11 026943 A (<br>29 January 1999 (19<br>* abstract; figures | -04-30)<br>KYOCERA CORP)<br>99-01-29)                                      |   | 1,17,23,<br>33                          |  |
| A   | PATENT ABSTRACTS OF<br>vol. 2000, no. 16,<br>-& JP 2001 015910 A<br>19 January 2001 (20<br>* abstract; figures                        | 2001-05-08)  | 19,20,<br>35-37   | TECHNICAL FIELDS<br>SEARCHED (Int.Cl.7) |  |
| A   | WO 94/07349 A (HUGH<br>31 March 1994 (1994<br>* claims; figures *   |  | 19-22,<br>35-37   |   |  |
| Α   | US 6 103 134 A (DUN<br>15 August 2000 (200<br>* column 4, line 19   | 0-08-15)   | }   | 19-22                                   |  |
|   | The present search report has   | been drawn up for all  | claims  |   |  |
|   | Place of search   |  | pletion of the search   |   | Examiner                                     |
|   | The Hague   | 3 May  | 2004  | Mes                                     | . L  |
| CATEGORY OF CITED DOCUMENTS  X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written discosure |   |  | T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding |   |  |

EPO FORM 1503 03.82 (P04C01)



Application Number

EP 02 25 3836

| CLAIMS INCURRING FEES  |
|--|
| The present European patent application comprised at the time of filing more than ten claims.  |
| Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):   |
| No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.   |
| LACK OF UNITY OF INVENTION   |
| The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:  |
| see sheet B  |
| All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.   |
| As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.  |
| Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims: |
| None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:                        |
|  |



# LACK OF UNITY OF INVENTION SHEET B

Application Number

EP 02 25 3836

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-18, 23-34

Double-sided or multilayered wiring boards with passive components by coating resistive paste and/or dielectric paste on metal foils; via connections by conical bumps penetrating through the substrate

2. claims: 19-22, 35-37

Magnetically permeable areas by magnetically permeable bumps or by filling holes with magnetically permeable material

# ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 02 25 3836

This annex lists the patent family members relating to the patent documents cited in the above–mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

03-05-2004

| Patent document<br>cited in search repor | t | Publication date |  | Patent family member(s)  |                                 | Publication date   |
|--|---|------------------|--|--|---------------------------------|--|
| US 4204187                               | A | 20-05-1980       | JP<br>JP<br>JP<br>BE<br>DE<br>FR<br>GB<br>NL<br>US | 1098569 C<br>54069768 A<br>56040514 B<br>871962 A<br>2847356 A<br>2408973 A<br>2007917 A<br>7811195 A<br>4368252 A                                   | l<br>l<br>,B                    | 27-05-198<br>05-06-197<br>21-09-198<br>01-03-197<br>17-05-197<br>08-06-197<br>23-05-197<br>16-05-198 |
| JP 08195561                              | Α | 30-07-1996       | NONE   |  |                                 |  |
| US 5920454                               | A | 06-07-1999       | NONE   |  |                                 |  |
| US 4870746                               | A | 03-10-1989       | CA   | 2002001 A  | 1                               | 07-05-199  |
| JP 02125692                              | Α | 14-05-1990       | JP<br>JP   | 1890638 C<br>6014580 B   |                                 | 07-12-199<br>23 <b>-</b> 02-199  |
| EP 0073904                               | A | 16-03-1983       | DE<br>AT<br>EP<br>JP                               | 3135554 A1<br>27671 T<br>0073904 A2<br>58056387 A  |                                 | 07-04-198<br>15-06-198<br>16-03-198<br>04-04-198   |
| EP 0409668                               | Α | 23-01-1991       | JP<br>JP<br>AT<br>DE<br>DE<br>EP                   | 2764745 B2<br>3054853 A<br>117869 T<br>69016296 D2<br>69016296 T2<br>0409668 A2  | 1                               | 11-06-199<br>08-03-199<br>15-02-199<br>09-03-199<br>10-08-199<br>23-01-199                           |
| JP 11026943                              | Α | 29-01-1999       | JP   | 3199664 B2   | 2                               | 20-08-200  |
| JP 2001015910                            | A | 19-01-2001       | NONE   |  |                                 |  |
| WO 9407349                               | A | 31-03-1994       | CA DE DK EP ES GR JP JP KR                         | 2124196 C<br>69312466 DT<br>69312466 TZ<br>613610 TZ<br>0613610 AZ<br>2105326 TZ<br>3024693 TZ<br>2509807 BZ<br>7501910 T<br>158475 BZ<br>9305885 AZ | 2<br>3<br>1<br>3<br>3<br>3<br>2 | 29-04-199 04-09-199 26-02-199 25-08-199 07-09-199 16-10-199 31-12-199 26-06-199 23-02-199 15-12-199  |

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

FORM P0459

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 02 25 3836

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03-05-2004

|    | Patent document<br>ed in search report |   | Publication date |                      | Patent family<br>member(s)                 |         | Publication date                                 |
|----|--|---|------------------|----------------------|--|---------|--|
| WO | 9407349                                | A |                  | WO<br>US             | 9407349<br>5438167                         | A1<br>A | 31-03-199<br>01-08-199                           |
| US | 6103134                                | Α | 15-08-2000       | EP<br>JP<br>TW<br>WO | 1062849<br>2002534816<br>465265<br>0041446 | T<br>B  | 27-12-200<br>15-10-200<br>21-11-200<br>13-07-200 |
|    |  |   |                  |                      |  |         |  |
|    |  |   |                  |                      |  |         |  |
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|    |  |   |                  |                      |  |         |  |
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82